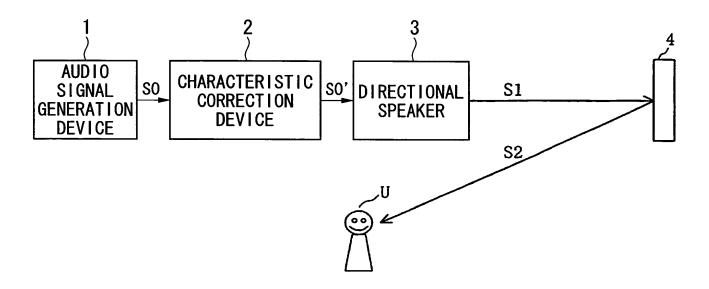
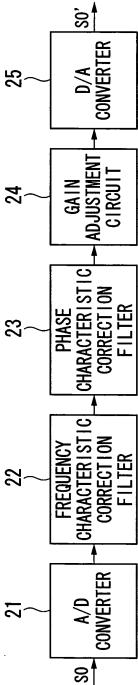
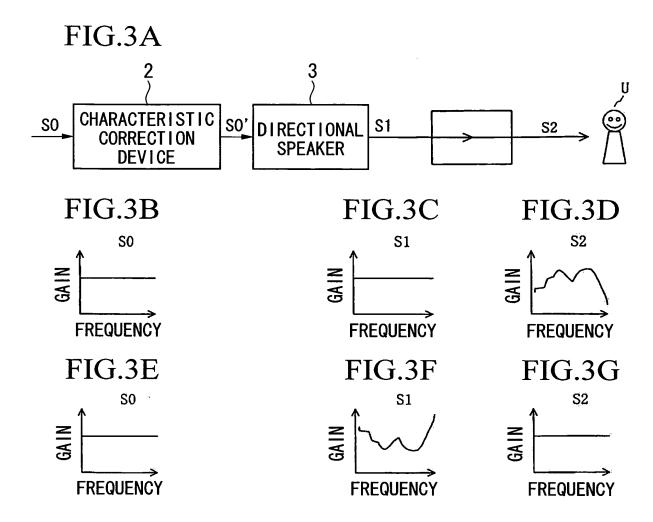
FIG.1









SO' DELAY CIRCUIT 32-n 33-n 34-n

FIG.5

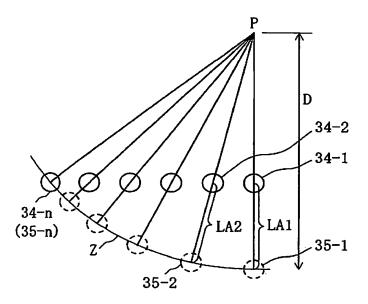


FIG.6

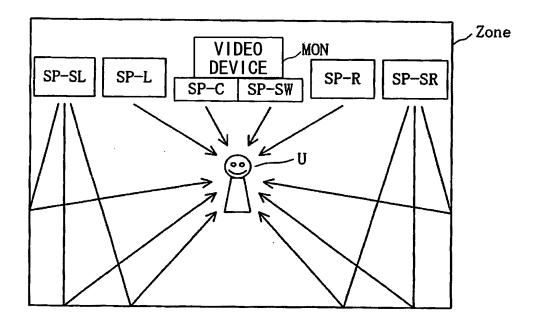
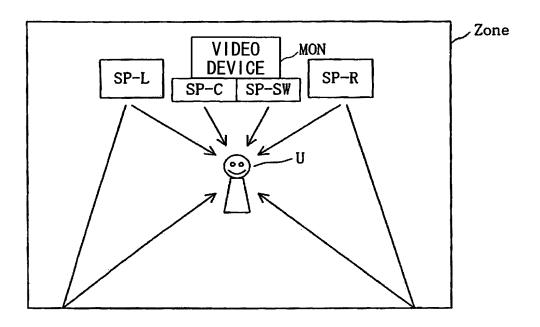
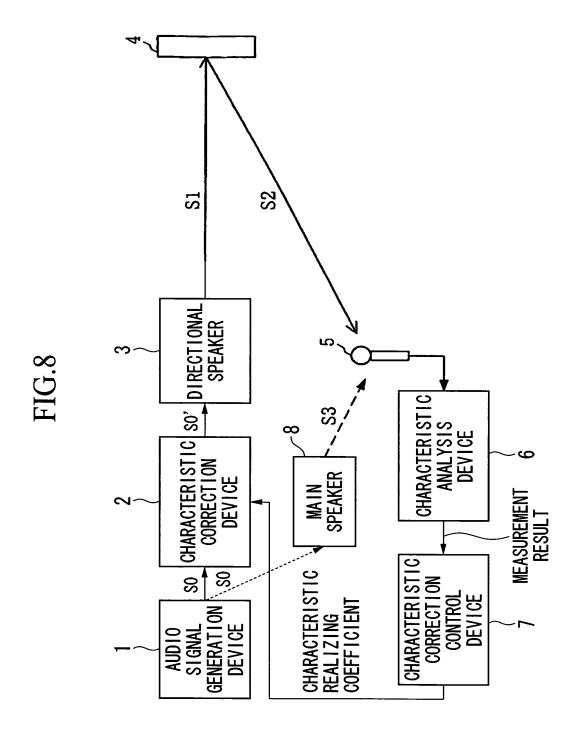
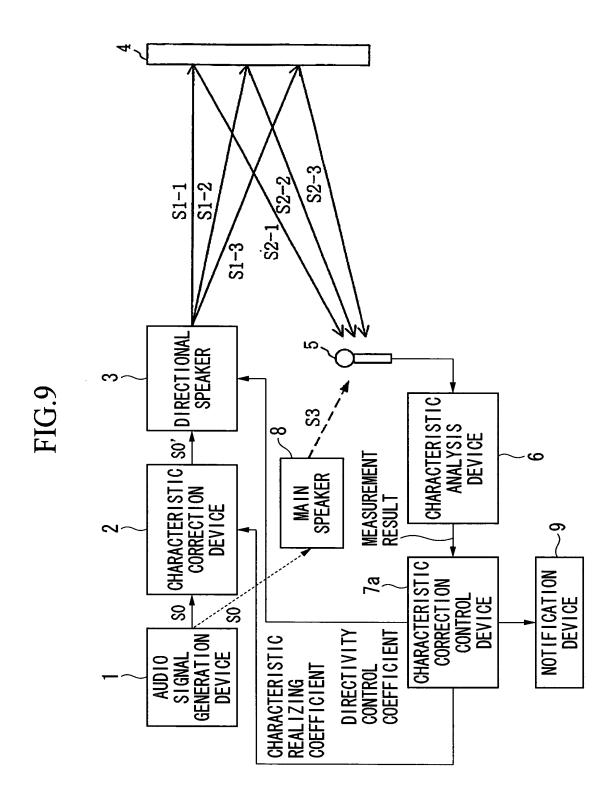


FIG.7







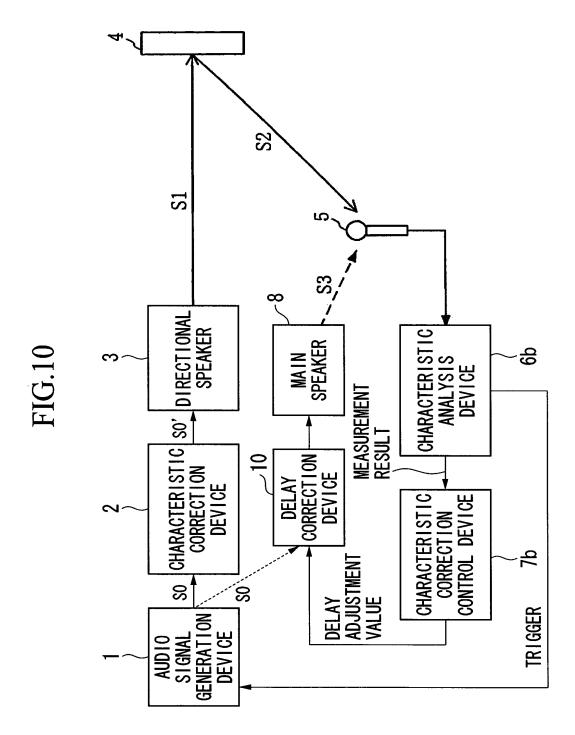
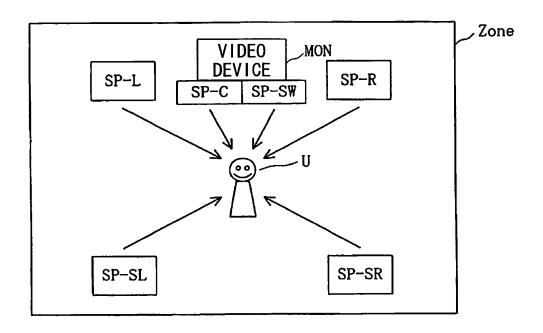


FIG.11



**FIG.12** 

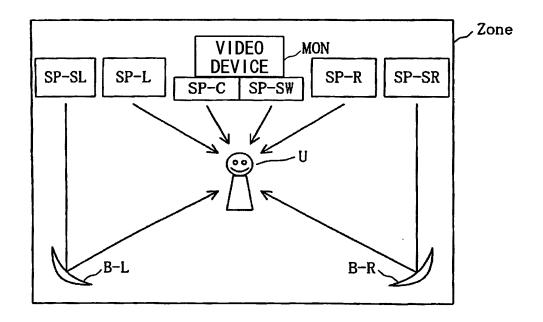


FIG.13

